Hw 14

1) V_{trip} @ $V_{in} = V_{out}$

$$= \frac{V_{Tn} + (V_{DD} + V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

$$V_{Trip} = \frac{0.4 + (3.0 - 0.4)\sqrt{\frac{250/3}{250}\cdot\frac{1}{1}}}{1 + \sqrt{\frac{250/3}{250}\cdot\frac{1}{1}}}$$

$$= 1.21 \text{ V}$$

$$V_{Trip} = \frac{0.4 + (3.0 - 0.4)\sqrt{\frac{250/3}{250}\cdot\frac{5}{1}}}{1 + \sqrt{\frac{250/3}{250}\cdot\frac{5}{1}}}$$

$$= 1.64 \text{ V}$$

2) Minimum sized k-input Nor gate

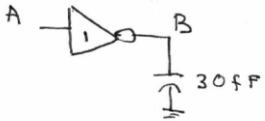
$$t_{prop} = \left(\frac{3k+1}{2}\right) t_{ref}$$

Minimum sized k-input NAND gate

$$t_{prop} = \left(\frac{3+k}{2}\right) t_{ref}$$

Problem 3

Assume $C_{REF} = 4fF$ $R_{P@REF} = 2.5K\Omega$



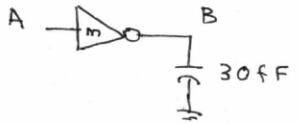
$$C_L = \frac{30fF}{4fF} = 7.5\,C_{REF}$$

$$t_{HL} = R_{P@REF} \cdot C_L = 7.5\,C_{REF} \cdot R_{P@REF}$$

$$t_{HL} = \frac{7.5}{2}\,t_{REF} = 3.75\,t_{REF}$$

but for $OD=1$, $t_{LH} = t_{HL}$

$\therefore\ t_{LH} = 3.75\,t_{REF}$



For minimum sized inverter

$$t_{HL} = \frac{t_{REF}}{2}\left(\frac{1}{OD_{HL}}\right) \cdot FI_{LOAD}$$

but $OD_{HL} = 1$, $FI_{LOAD} = 7.5$

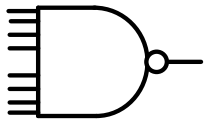
$\therefore\ t_{HL} = 3.75\,t_{REF}$

and $OD_{LH} = \frac{1}{3}$

$$t_{LH} = t_{\frac{REF}{2}}\left(\frac{1}{OD_{LH}}\right) \cdot FI_{LOAD}$$

$\therefore\ t_{LH} = 11.25\,t_{REF}$

Problem 4 For all inputs, L=Lmin.



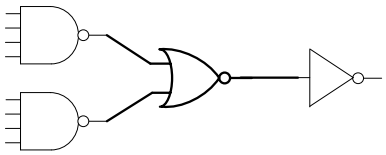
$W_n=8W_{min}$, $Wp=3W_{min}$ so the capacitance on each input is

$$C_{IN} = C_{OX}\left(W_n L_n + W_p L_p\right) = C_{OX} L_{MIN}\left(W_n + W_p\right) = C_{OX} L_{MIN}\left(11W_{MIN}\right)$$

But $C_{REF}=4C_{OX}W_{MIN}L_{MIN}$ so $C_{IN} = \frac{11}{4} C_{REF}$

Since there are 8 total inputs, the total gate area is

$$A_{GATE} = 8 \bullet \left(L_{MIN} \bullet 8W_{MIN} + L_{MIN} \bullet 3W_{MIN}\right) = 88 L_{MIN} W_{MIN}$$



For the inputs on the 4-input NAND gates, $W_n=4W_{min}$, $Wp=3W_{min}$ so the capacitance on each input is

$$C_{IN} = C_{OX}\left(W_n L_n + W_p L_p\right) = C_{OX} L_{MIN}\left(W_n + W_p\right) = C_{OX} L_{MIN}\left(7W_{MIN}\right)$$

But $C_{REF}=4C_{OX}W_{MIN}L_{MIN}$ so $C_{IN} = \frac{7}{4} C_{REF}$

Since there are 8 inputs at the first level of logic, the gate area at the first level of logic is

$$A_{GATE1} = 8 \bullet \left(L_{MIN} \bullet 4W_{MIN} + L_{MIN} \bullet 3W_{MIN}\right) = 56 L_{MIN} W_{MIN}$$

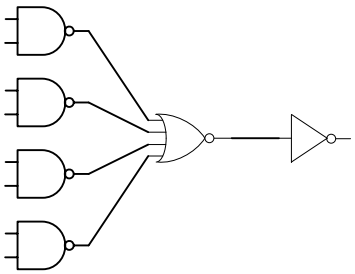
At the second level of logic, the 2-input NOR gate will have $W_n=W_{MIN}$ and $W_P=6W_{MIN}$ so the gate area at the second level of logic is

$$A_{GATE2} = 2 \bullet \left(L_{MIN} \bullet W_{MIN} + L_{MIN} \bullet 6W_{MIN}\right) = 14 L_{MIN} W_{MIN}$$

And at the third level of logic, the inverter will have a gate area of

$$A_{GATE3} = \left(L_{MIN} \bullet W_{MIN} + L_{MIN} \bullet 3W_{MIN}\right) = 4 L_{MIN} W_{MIN}$$

So the total gate area is $A_{TOTAL} = \sum_{i=1}^{3} A_{GATEi} = 74 L_{MIN} W_{MIN}$



For the inputs on the 2-input NAND gates, $W_n=2W_{min}$, $Wp=3W_{min}$ so the capacitance on each input is $C_{IN} = C_{OX}\left(W_n L_n + W_p L_p\right) = C_{OX} L_{MIN}\left(W_n + W_p\right) = C_{OX} L_{MIN}\left(5W_{MIN}\right)$

But $C_{REF}=4C_{OX}W_{MIN}L_{MIN}$ so $C_{IN} = \frac{5}{4} C_{REF}$

Since there are 8 inputs at the first level of logic, the gate area at the first level of logic is

$$A_{GATE1} = 8 \bullet \left(L_{MIN} \bullet 2W_{MIN} + L_{MIN} \bullet 3W_{MIN} \right) = 40 L_{MIN} W_{MIN}$$

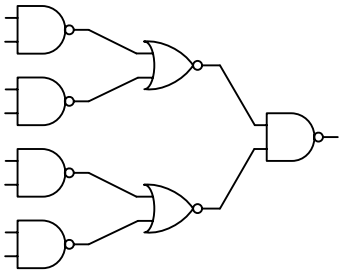
At the second level of logic, the 4-input NOR gate will have $W_n=W_{MIN}$ and $W_P=12W_{MIN}$ so the gate area at the second level of logic is

$$A_{GATE2} = 4 \bullet \left(L_{MIN} \bullet W_{MIN} + L_{MIN} \bullet 12W_{MIN} \right) = 52 L_{MIN} W_{MIN}$$

And at the third level of logic, the inverter will have a gate area of

$$A_{GATE3} = \left(L_{MIN} \bullet W_{MIN} + L_{MIN} \bullet 3W_{MIN} \right) = 4 L_{MIN} W_{MIN}$$

So the total gate area is $A_{TOTAL} = \sum_{i=1}^{3} A_{GATEi} = 96 L_{MIN} W_{MIN}$



For the inputs on the 2-input NAND gates, $W_n=2W_{min}$, $Wp=3W_{min}$ so the capacitance on each input is $C_{IN} = C_{OX} \left(W_n L_n + W_p L_p \right) = C_{OX} L_{MIN} \left(W_n + W_p \right) = C_{OX} L_{MIN} \left(5W_{MIN} \right)$

But $C_{REF}=4C_{OX}W_{MIN}L_{MIN}$ so $C_{IN} = \frac{5}{4} C_{REF}$

Since there are 8 inputs at the first level of logic, the gate area at the first level of logic is

$$A_{GATE1} = 8 \bullet \left(L_{MIN} \bullet 2W_{MIN} + L_{MIN} \bullet 3W_{MIN} \right) = 40 L_{MIN} W_{MIN}$$

At the second level of logic, the 2-input NOR gate will have $W_n=W_{MIN}$ and $W_P=6W_{MIN}$ so the gate area at the second level of logic is

$$A_{GATE2} = 4 \bullet \left(L_{MIN} \bullet W_{MIN} + L_{MIN} \bullet 6W_{MIN} \right) = 28 L_{MIN} W_{MIN}$$

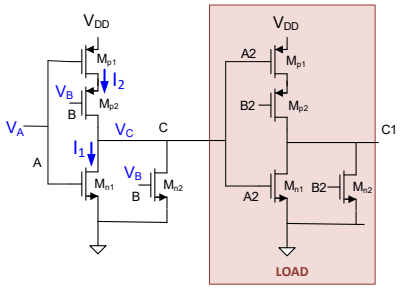
And at the third level of logic, the NAND gate will have a gate area of

$$A_{GATE3} = 2 \bullet \left(L_{MIN} \bullet 2W_{MIN} + L_{MIN} \bullet 3W_{MIN} \right) = 10 L_{MIN} W_{MIN}$$

So the total gate area is $A_{TOTAL} = \sum_{i=1}^{3} A_{GATEi} = 78 L_{MIN} W_{MIN}$

Problem 5 For a k-input NOR gate with k=3, if OD=1 and equal to that of the reference inverter $L_n=L_p=L_{min}$, $W_n=W_{min}$ and $W_p=3kW_{min}=9W_{min}$

Problem 6 Circuit is shown below but trip point determined by the input gate only, not affected by the Load.



There are two scenarios that cause the output to transition. One is when one of the inputs transitions and the other input is low. The other is when both inputs transition together. We will denote these as Case 1 and Case 2.

a) Case 1. Assume B input is 0 and A input transitions between 0 and 1. If the B input is 0, Mn2 is in cutoff. Trip point will occur when VA=VC and this will happen when Mn1 and MP1 are in Sat region. Since Mn1 and Mp1 are in saturation,

$$I_1=\frac{\mu_n C_{OX} W_{n1}}{2L_{n1}}\left(V_A-V_{THn}\right)^2$$

$$I_2=\frac{\mu_p C_{OX} W_{p1}}{2L_{p1}}\left(V_A-V_{DD}-V_{THp}\right)^2$$

Equating these two currents and solving for VA, obtain

$$V_A=V_{TRIP}=\frac{\left(V_{THn}\right)+\left(V_{DD}+V_{THp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_{p1}}{W_{n1}}\frac{L_{n1}}{L_{p1}}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_{p1}}{W_{n1}}\frac{L_{1n}}{L_{p2}}}}$$

Case 2 Assume A and B inputs are connected together. In this scenario, Mn1 and Mn2 are connected in parallel and serve as a single device with effective width equal to 2Wn1. Again, trip point will occur when VA=VC and this will happen when the parallel combination of MN1 and MN2 is in saturation and when MP1 is in saturation. We thus have

$$I_1=\frac{\mu_n C_{OX} 2W_{n1}}{2L_{n1}}\left(V_A-V_{THn}\right)^2$$

$$I_2=\frac{\mu_p C_{OX} W_{p1}}{2L_{p1}}\left(V_A-V_{DD}-V_{THp}\right)^2$$

Equating these two currents and solving for VA, obtain

$$V_A=V_{TRIP}=\frac{\left(V_{THn}\right)+\left(V_{DD}+V_{THp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_{p1}}{2W_{n1}}\frac{L_{n1}}{L_{p1}}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_{p1}}{2W_{n1}}\frac{L_{1n}}{L_{p2}}}}$$

b) Since the first NOR gate is driving an identical device, the load on the first stage has a Fan-in of $\mathbf{FI}_{LOAD}=\left.\left(\frac{\mathbf{3k+1}}{\mathbf{4}}\right)\right|_{k=2}=\frac{7}{4}.$ For a two-input NOR gate, there is only a single LH output transition (there are two HL output transitions) and since the gates are sized for equal worst-case rise-fall times, $t_{LH}=\frac{t_{REF}}{2}\bullet \mathrm{FI}_{LOAD}=\frac{7}{8}t_{REF}$

Problem 7

Since sized for equal worst-case rise-fall times with OD=1, we have $\mathbf{t_{PROP} = t_{REF} \bullet \sum_{k=1}^{3} F_{I(k+1)}}$

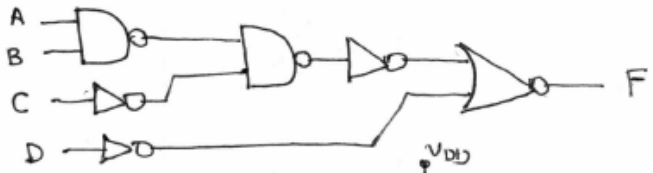
It follows that $F_{I2} = \left.\frac{3+k}{4}\right|_{k=3} = \frac{3}{2}$ $F_{I3} = \left.\frac{3k+1}{4}\right|_{k=2} = \frac{7}{4}$ $F_{I4} = \left.\frac{20fF}{C_{REF}}\right|_{CREF=4fF} = 5$

Thus $t_{PROP}=8.25t_{REF}$.

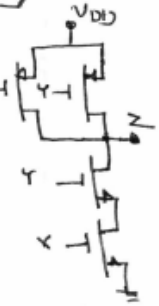
Problem 8. There are multiple solutions. One follows.

$\overline{F} = (\overline{AB} \cdot \overline{C}) + \overline{D}$

Gate Implementation



For NAND gates:

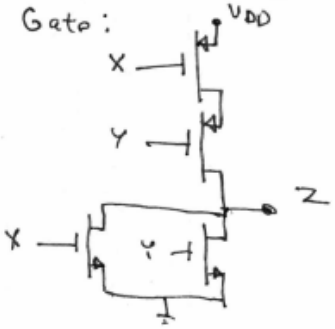


$L_n = L_p = L_{min}$

$w_n = 2w_{min}$

$w_p = 3w_{min}$

For NOR Gate:

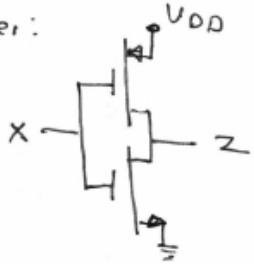


$L_n = L_p = L_{min}$

$w_n = w_{min}$

$w_p = 6w_{min}$

For Inverter:

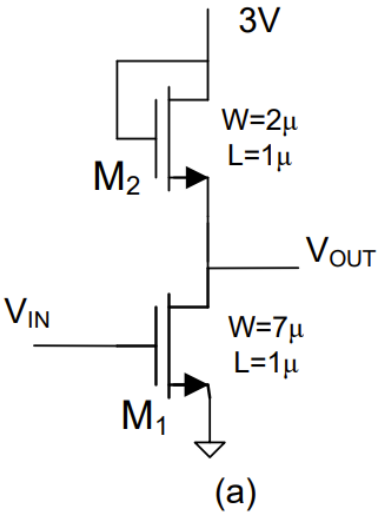


$L_n = L_p = L_{min}$

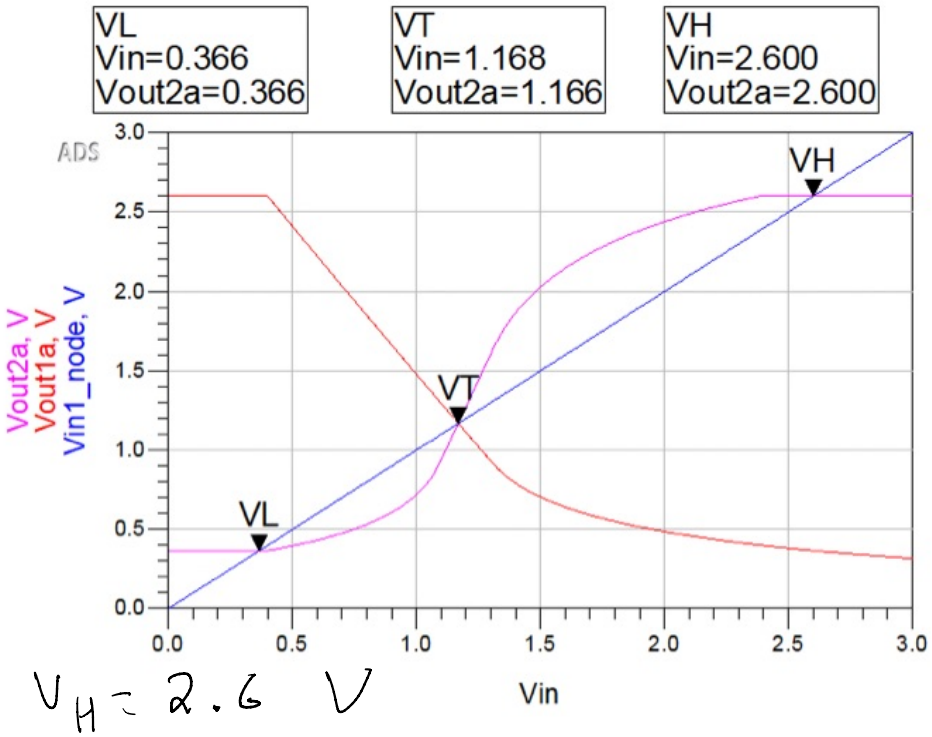
$w_n = w_{min}$

$w_p = 3w_{min}$

9)

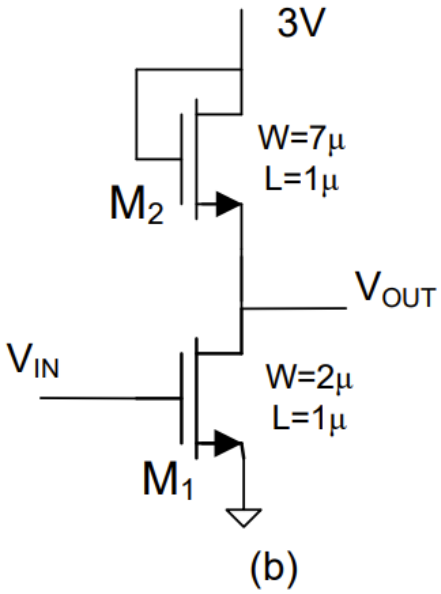


(a)

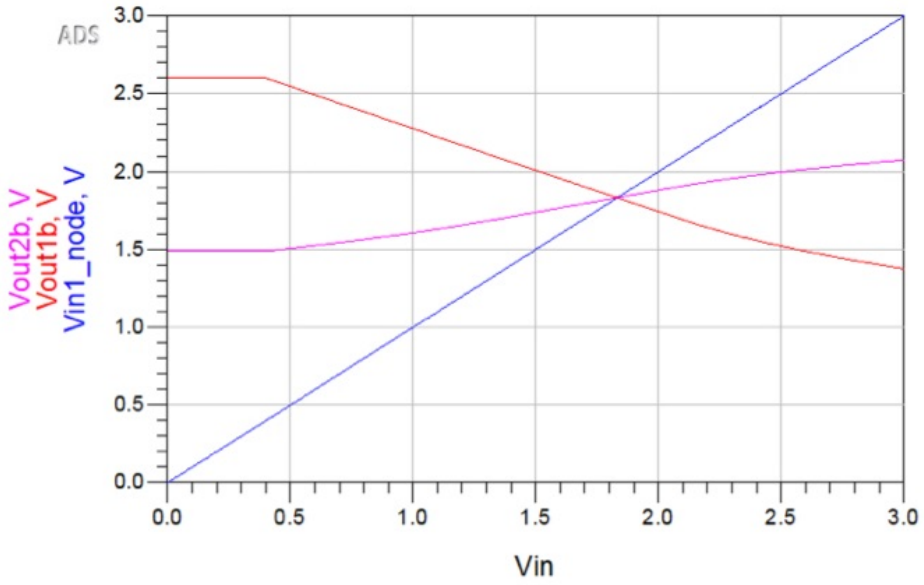


$V_L = 366\ mV$

$V_H = 2.6\ V$

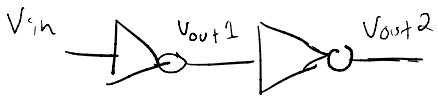


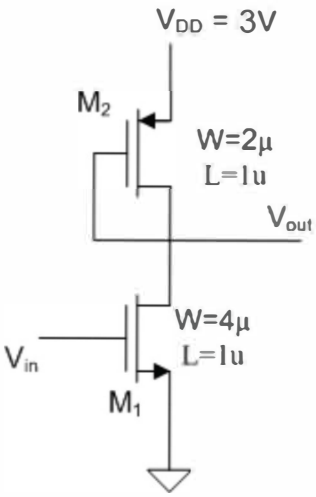
(b)



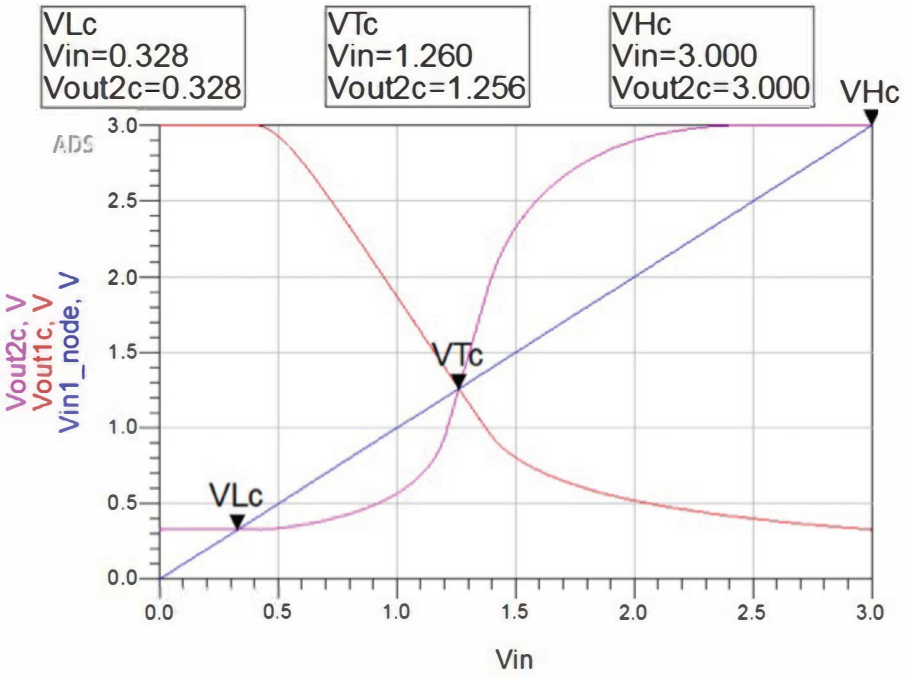
Not an inverter

Using simple Mosfet model





(c)



$V_L = 328$ mV

$V_H = 3$ V